

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
10 October 2002 (10.10.2002)

PCT

(10) International Publication Number
WO 02/080353 A2

(51) International Patent Classification⁷: **H03F 3/217**

(21) International Application Number: PCT/GB02/01473

(22) International Filing Date: 27 March 2002 (27.03.2002)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
0108076.1 30 March 2001 (30.03.2001) GB

(71) Applicant: **1...LIMITED** [GB/GB]; St John's Innovation Centre, Cowley Road, Cambridge CB4 0WS (GB).

(72) Inventors; and

(75) Inventors/Applicants (for US only): **HOOLEY, Anthony** [GB/GB]; 79 De Freville Avenue, Cambridge CB4 1HP (GB). **WINDLE, Paul, Raymond** [GB/GB]; 10 Blacklands Close, Saffron Walden, Essex CB11 4BX (GB).

(74) Agents: **MERRYWEATHER, Colin, Henry et al.**; J.A. Kemp & Co., 14 South Square, Gray's Inn, London WC1R 5JJ (GB).

(81) Designated States (national): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZM, ZW.

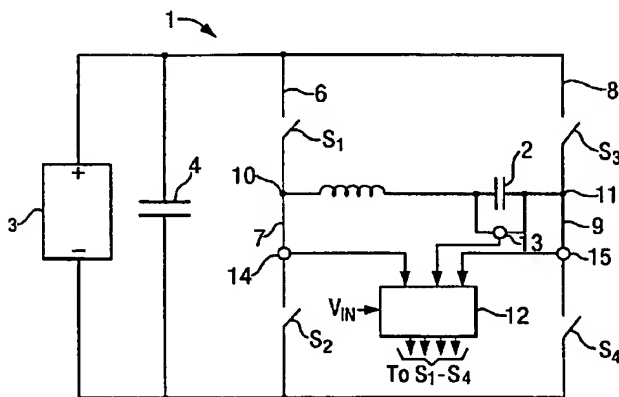
(84) Designated States (regional): ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— without international search report and to be republished upon receipt of that report

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: CAPACITIVE POWER DRIVER CIRCUIT



(57) Abstract: A capacitive power driver circuit (1) for driving an output signal on a capacitive load (2) in accordance with an input signal. The output signal may be the voltage across the load (2) or the charge stored on the load. The driver circuit (1) comprises a bridge arrangement of switchable current paths which constitute a bipolar charging circuit for charging the load (2) from a power supply unit (3) and a discharge circuit for discharging the load (2). An inductor (5) is provided in series with the load (2). The driver circuit (1) includes a detector (13) for detecting the output signal on the load (2) and current sensors (14, 15) for detecting the charging and discharge currents. A controller (12) controls switching of the charging circuit and the discharge circuit to drive the output signal in accordance with the input signal. During charging of the load (2), the driver circuit (1) switches alternately between closing the charging circuit and opening the charging circuit while at the same time closing the discharge circuit to provide a path for the charging current driven by the inductor (5). During discharge of the load, the driver circuit (1) switches alternately between closing the discharge circuit and opening the discharge circuit while closing the charging circuit for the discharge current to be driven by the inductor (5) into the power supply unit (3) against the output potential of the power supply unit (3).



WO 02/080353 A2

CAPACITIVE POWER DRIVER CIRCUIT

The present invention relates to a capacitive power driver circuit for driving a capacitive load. In particular the driver circuit drives an output signal on the load in accordance with an input signal. The present invention is applicable for driving any type of capacitive load, although it is particularly suitable for driving a capacitive load in the form of an electrostatic loudspeaker or in the form of a piezoelectric or other electro-active device.

Power driver circuits for driving a specific load such as a loudspeaker, an antenna, a motor, or indeed any load that requires a significant power are usually based around a power amplifier. Power amplifiers of many types are known. The majority of such power amplifiers are classifiable as either voltage amplifiers or current amplifiers. The former nominally produce a specific output load voltage in accordance with an input signal independent of the actual value of the load (within operating limits). The latter nominally produce a specific output load current in accordance with the input signal independent of the actual value of the load (within operating limits). Thus voltage amplifiers can usefully be described as low output impedance devices and current amplifiers as high output impedance devices, but in both cases the nominal output impedance of the power amplifier is resistive. This has an immediate consequence on the relative power dissipated in the power amplifier and the load.

If efficiency η is defined as the ratio of the energy delivered to the load to the sum of the energy delivered to the load plus the energy lost in the driver circuit, then in the case that the load is substantially resistive, it can be shown that the maximum possible efficiency η is $R_L/(R_L + R_O)$, where R_L is the resistance of the load and R_O is the output resistance of the power amplifier. For many types of power amplifier, for example Class A power amplifiers, there is quiescent power dissipation resulting in low efficiency even when the output impedance R_O of the power amplifier is low. High efficiencies are important so that the majority of the power developed by the power amplifier is dissipated usefully in the load and not wasted as heat in the power

-2-

amplifier itself. High efficiencies can be achieved by ensuring that the output resistance of the power amplifier is substantially below the resistance of the load.

However, such high efficiency is not possible in the case that the load is substantially reactive, whether predominantly inductive or capacitive. In this case, the result of the reactive component of the impedance of the load is that the voltage V_T across the output terminals of the power amplifier (that is the drive voltage across the load) will be different in phase from the output current I_O flowing through both the load and the internal resistance of the power amplifier. For a substantially reactive load in which the magnitude of the reactance of the load is substantially greater than the resistance of the load at the frequencies of interest, the phase of the terminal voltage V_T may be almost in quadrature with the phase of the output current I_O . In addition, it can no longer be assume that the resistance of the load is substantially greater than the output resistance of the amplifier. Under such load conditions it may be that the resistance of the load is substantially less than the output resistance of the power amplifier, even when by proper design of the power amplifier the magnitude of the reactance of the load is substantially greater than the output resistance of the power amplifier.

The result of these factors are that the efficiency η , that is the ratio of the power dissipated in the load to the total power dissipated, becomes very low with a substantially reactive load. This results from the quadrature relationship between the output EMF voltage V_O and the terminal voltage V_T of the power amplifier. This means that the magnitude of the voltage across the output resistance of the power amplifier becomes a significant fraction of the magnitude of the output EMF voltage V_O . This gives rise to a large internal power dissipation in the power amplifier.

To give a practical example, consider a typical circuit for a piezoelectric device having a load impedance comprised of a capacitance of 102.5nF in series with a resistance of 0.26 Ω , driven by a 142.8V peak sine-wave of frequency 10kHz from a power amplifier with output resistance 0.1 Ω . In this typical example, it can be shown that the efficiency is of the order of 0.16%. This is despite the power amplifier having a seemingly low output impedance (0.1 Ω) which is in fact largely

-3-

immaterial because of the almost quadrature phase angle between the terminal voltage V_T and the current I_O .

The present invention tackles the problem that the efficiency of a power driver circuit using a power amplifier is low when driving a load which is capacitive.

5 The present inventors have considered forming a power driver circuit as a simple switching driver in which the load is charged and discharged through switched circuits. In this case, there will be dissipation of energy in the residual resistance in the charging and discharge circuits, for example the resistance of the switches used to switch the circuits. The energy dissipated during charging of the
10 capacitive load of capacitance C to a peak voltage V_p may be shown to be equal to the peak energy E_p stored in the load, that is a $\frac{1}{2}CV_p^2$. Similarly, the energy dissipated in the residual resistance in the circuit during discharge of the capacitor is also equal to this same value. This result may be shown by integrating the instantaneous power P dissipated in the residual resistance which power is equal to
15 I^2R , where R is the residual resistance and I is the current which falls exponentially with a time constant equal to RC . The dissipated energy is independent of the value of the residual resistance R . Therefore the same energy is dissipated no matter how low (or high) this resistance R is.

 Thus, the total energy dissipated in charging and discharging the capacitor is
20 equal to twice the peak amount of energy stored on the capacitor. Therefore, even with an ideal switching power driver the maximum achievable efficiency is $33\frac{1}{3}\%$. Considering a sinusoidal drive voltage with frequency f , the rate of power dissipation is therefore $4fE_p$ where E_p is the peak energy stored on the capacitive load. This power has to be supplied by the power driver circuit and is dissipated as heat.

25 In summary, in a linear power amplifier, supplying energy to a capacitive load is a very inefficient process and results in extremely high energy dissipation in the power amplifier. Even in a conventional switching driver circuit, at least as much energy as the peak energy stored on the capacitive load is lost in each quarter cycle. If efficiency is defined as before as the ratio of the energy delivered to the load to the
30 sum of the energy delivered to the load plus the energy dissipated in the driver

-4-

circuit, then such a switching driver has a maximum attainable efficiency of only 33⅓%. Whilst this is an improvement over a linear power amplifier, it is still very wasteful of energy.

The purpose of the present invention is to provide a power driver circuit with improved efficiency.

According to the present invention, there is provided a capacitive power driver circuit for driving an output signal on a capacitive load in accordance with an input signal, the driver circuit comprising: a switchable charging circuit for charging the load from a power supply unit; a switchable discharge circuit for discharging the load; an inductor in series with the load in the charging circuit and the discharge circuit; means for deriving a measure of the output signal on the load; and a controller, responsive to the input signal and the output signal detected by the detector, for controlling switching of the charging circuit and discharge circuit to drive the output signal in accordance with the input signal.

The use of an inductor serves to improve the efficiency of the power driver circuit as compared to a simple switched driver circuit. The capacitive power drive circuit of the present invention is distinguished over a simple switched driver circuit by the provision of an inductor in series with the load, in both the charging circuit and the discharge circuit. Accordingly, charging and discharging occur through the inductor. The inductor serves to limit the current flowing in the charging and discharge circuits during charging and discharging of the load. To be specific, the inductance limits the rate of change of current. The controller may thus, by appropriate control of the timing of the switching of the charging and discharge circuit, limit the peak current flowing in the charging and discharge circuits. If the peak current is limited during charging and discharge of the capacitive load, the energy dissipated in the residual resistance R_s of the driver circuit, for example the resistance of the switches for opening and closing the charging and discharge circuits, will be similarly limited. This is because the power dissipated in the residual resistance is proportional to the square of the current. Of course, whilst some power loss is inevitable, the present invention provides a higher efficiency

-5-

driver power driver circuit than is achievable with a simple switched driver circuit. In practice an efficiency of well over 90% is achievable, as compared to a maximum efficiency of 33⅓% for a simple switched driver circuit, as described above.

Preferably, the driver circuit further comprises at least one current sensor for
5 detecting the current flowing into and out of the load, and the controller is responsive to the current detected by the at least one current sensor to control said switching.

The use of current sensors is a simple and effective way for the controller to control switching of the charging and discharge circuits to limit the peak current flowing, because the controller can effect switching when the current reaches
10 predetermined levels. However this is not essential, as the controller could instead effect switching at predetermined timings.

Preferably, the controller is arranged during charging of the load to switch alternately between: closing the charging circuit; and opening the charging circuit while closing the discharge circuit to provide a path for the charging current driven
15 by the inductor.

As a result, by alternately switching between opening and closing of the charging circuit, the effect of the controller is to limit the peak current flowing during charging of the load. Hence the amount of wasted power dissipated in the residual resistance of the driver circuit is limited. When the charging circuit is opened, the
20 inductor will continue to drive charging current because the current flowing through an inductor cannot be changed instantaneously. Accordingly, at this time the discharge circuit is closed to provide a path for the charging current driven by the inductor. As a result, after opening of the charging circuit the capacitive load will continue to be charged, but the charging current will decay. Subsequently the
25 charging circuit will be closed once again causing the charging current to rise again. In this way, the charging current may be cycled up and down. During each cycle, energy is transferred from the power supply unit to the inductor which stores the energy in the form of internal magnetic fields and subsequently to the load. By this mechanism energy wastage is reduced.

30 The charging circuit may be opened in response to the magnitude of the

-6-

charging current rising to a predetermined maximum charging current. Similarly the charging circuit may be closed in response to the charging current falling to a predetermined minimum charging current. The maximum and minimum charging currents may be detected by one or more current sensors. However, this is not
5 essential, as a similar control could be effected simply by the controller controlling switching at predetermined timings. In this case, the timings would be selected to limit the peak current flowing based on the known value of the inductor, the expected capacitive load and the expected frequency range of the input signal.

Preferably, the controller is arranged during charging of the load to maintain a
10 positive charging current.

Preferably, the controller is arranged during discharging of the load to switch alternately between: closing the discharge circuit; and opening the discharge circuit while closing the charging circuit for the discharge current to be driven by the inductor into the power supply unit against the output potential of the power supply
15 unit.

The effect of the control performed by the controller is as follows. Closing the discharge circuit causes the load to be discharged. The rate of rise of the discharge current is limited by the inductance of the inductor. By alternating from closing of the discharge circuit to opening of the discharge circuit, the current
20 flowing is limited. Thus the power dissipated in the residual resistance of the driver circuit is similarly limited. When the discharge circuit is opened, the inductor continues to drive current flow, because it is not possible to instantaneously change the current flowing through an inductor. Accordingly, by closing the charging circuit this provides a path for the discharge current to be driven into the power supply unit.
25 This occurs against the potential of the power supply unit. This is possible because the nature of an inductor is that it will generate a sufficiently high terminal voltage to maintain the current flowing through it. Therefore the inductor generates sufficient terminal voltage to overcome the output potential of the power supply unit. Thus the effect is for energy to be fed back into the power supply unit. In other words, the
30 present invention provides a driver circuit in which energy stored on the capacitive

-7-

load may be fed back to the power supply unit instead of being dissipated in the discharge circuit and hence wasted.

After opening the discharge circuit, the discharge current driven by the inductor will decay until the controller alternates back to closing the discharge
5 circuit. In this way the discharge current will cycle up and down. During each cycle energy is transferred from the capacitive load to the inductor which stores the energy in the form of internal magnetic fields, and subsequently the energy stored in the inductor is forced back into the power supply unit. By this mechanism, energy wastage in the power driver circuit is reduced.

10 Closing of the discharge circuit may occur in response to the magnitude of the discharge current rising to a predetermined maximum discharge current. Similarly, opening of the discharge circuit may occur in response to the discharge current falling to a predetermined minimum discharge current. The maximum and minimum discharge currents may be detected by one or more current sensors to
15 which the controller is responsive. However, this is not essential, as the controller could instead be arranged to switch at predetermined timings selected based on the known value of the inductor, the expected capacitive load and the expected frequency range of the input signal.

Preferably, the controller is arranged during discharging of the load to
20 maintain a positive discharge current.

Many possible layouts of the driver circuit are possible to form the charging circuit and the discharge circuit. In many layouts, the charging circuit and the discharge circuit will be formed at least in part by common paths and components. Desirably, the charging circuit is a bipolar circuit for selectively charging the load
25 from the power supply unit in either polarity. Such a bipolar circuit allows the dynamic range of the output voltage to be upped to twice that achievable if the load may be charged by the power supply unit in one polarity only.

In the preferred layout, the charging circuit comprises a bridge arrangement of four paths around the series arrangement of the inductor and the load, the first and
30 second paths switchable connecting respective outputs of the power supply unit to

-8-

one end of the series arrangement of the inductor and the load and the third and fourth paths switchable connecting respective outputs of the power supply unit to the other end of the series arrangement of the inductor and the load, whereby the first and fourth paths comprise a charging path for charging the load with one polarity and the
5 second and third paths comprise a charging path for charging the load with the opposite polarity. In this case, for simplicity two of the four paths connected to the same output of the power supply unit are switchable connected together to form the discharge circuit.

The detector may be arranged to detect the output signal as the voltage across
10 the load. In this case, the controller will drive the voltage across the load in accordance with the input signal.

As an alternative, the detector may be arranged to detect the output signal as the charge stored by the load. For example, this may be achieved by the detector including a current sensor for detecting the current flowing into and out of the load
15 and means for integrating the detected current to derive the charge stored by the load. This causes the controller to drive the charge stored on the capacitive load as the output signal in accordance with the input signal. This is particularly advantageous when it is desired to drive a capacitive load which has a response which is non-linear with voltage but linear with charge, or which exhibits hysteresis. An example of
20 such a capacitive load is a piezoelectric or other electro-active device.

Many such electro-active devices have responses which are non-linear with voltage, for example due to hysteresis, over a desired operating range. In particular, the displacement is non-linear with voltage. However, the displacement is linear with the charge stored on the electro-active device. Therefore, when it is desired to
25 drive the displacement of the electro-active device in accordance with an input signal, this may be achieved by the present invention by driving the charge stored by the electro-active device. This aspect of the present invention is equally applicable to a power driver circuit in which no inductor is provided. Therefore, in accordance with a second aspect of the present invention, there is provided a capacitive power
30 driver circuit for driving an output signal on a capacitive load in accordance with an

-9-

input signal, the driver circuit comprising: a switchable charging circuit for charging the load from a power supply unit; a switchable discharge circuit for discharging the load; a detector for detecting the charge stored by the load as the output signal on the load; and a controller, responsive to the input signal and the output signal detected by the detector, for controlling switching of the charging circuit and discharge circuit to drive the output signal in accordance with the input signal.

To allow better understanding, preferred embodiments of the present invention will now be described by way of non-imitative example with reference to the accompanying drawings in which:

Fig. 1 is a circuit diagram of a capacitive power driver circuit in accordance with the present invention;

Fig. 2 is a graph of voltage and current during charging of the load;

Fig. 3 is a graph of voltage and current during discharge of the load;

Fig. 4 is a flow chart of the control algorithm performed by the controller;

and

Figs. 5 and 6 are circuit diagrams of respective capacitive power driver circuits which are alternatives to that of Fig. 1.

Fig. 1 is a circuit diagram of a capacitive power driver circuit 1 which drives a capacitive load 2. The load 2 may be any load which is capacitive. The load 2 may have a pure capacitance for which the associated resistance and inductance are negligible. However, the driver circuit 1 may be equally used with a load 2 which is dominantly capacitive but also has significant series and/or parallel resistance and/or inductance. The load 2 may be of numerous types. For example, the load 2 may be a piezoelectric or other electro-active device which might have a typical capacitance in the range 1nF to 10 μ F, or might be an electrostatic loudspeaker. The load 2 might equally be any other type of capacitive load. A wide range of possible capacitances may be accommodated by suitable sizing of the other components in the drive circuit 1.

The driver circuit 1 includes a dc power supply unit (PSU) 3 for charging the load 2. A reservoir capacitive 4 is provided in parallel with the PSU 3 although this

-10-

is optional, or may be an integral part of the PSU 3.

The driver circuit 1 includes an inductor 5 in a series with the load 2. Accordingly charging and discharge of the load 2 occur through the inductor 5. The inductance of inductor 5 limits the rate of change of the charge and discharge
5 currents. As the present invention involves the inductor 5 storing energy (as described in more detail below), the inductor 5 is preferably of a type having an insignificant energy loss for example with an air gap provided in the core.

The driver circuit 1 further includes a bridge arrangement of four switched paths 6 to 9 around the series arrangements of the inductor 5 and the load 2. The
10 switched paths 6 to 9 together constitute a bipolar charging circuit for charging the load 2 from the PSU 3 and also a discharge circuit for discharging the load 2.

In particular, the first path 6 and the second path 7 connect the positive and negative outputs, respectively, of the PSU 3 to the node 10 at one end of the series arrangement of the inductor 5 and the load 2. The third path 8 and the fourth path 9
15 connect the positive and negative outputs, respectively, of the PSU 3 to the node 11 at the other end of the series arrangement of the inductor 5 and the load 2. The four paths 6 to 9 each include a respective switch S_1 to S_4 for switchably opening and closing the respective paths 6 to 9. As a result of this bridge arrangement, the first path 6 and the fourth path 9 together form a first charging circuit charging the load 2
20 with a positive polarity, the first charging circuit being closed by closing the switches S_1 and S_4 . Similarly, the second path 7 and the third path 8 together comprises a second charging circuit for charging the load 2, but with the opposite, negative polarity, the second charging circuit being closed by closing the switches S_2 and S_3 . Also, the second path 7 and the fourth path 9 which are both connected to the
25 negative output of the PSU 3 together comprise a discharge circuit for discharging the load 2, the discharge circuit being closed by closing the switches S_2 and S_4 .

The switches S_1 to S_4 may be any suitable types of switch, for example transistors (FETS or bipolar transistors), thyristors (triacs where there is bidirectional current), or even relays where the load 2 demands such large scale circuitry. As a
30 protective measure, the switches S_1 to S_4 are preferably provided in a conventional

-11-

manner with reverse-biased diodes in case of transient reverse voltages being developed during switching of the driver circuit 1 from one state to another.

The switches S_1 to S_4 are each controlled by a controller 12 which thereby controls switching of the drive circuit 1 to opening and closing the charging circuit
5 and the discharge circuit formed by the four paths 6 and 9.

The driver circuit 1 further includes a detector 13 arranged to detect the voltage across the load 2. In this driver unit 1 the voltage across the load 2 is taken as the output signal so the detector 13 serves as a means for deriving a measure of the output signal on the load. The voltage detector 13 may be any suitable voltage
10 detector, although it preferably has good common mode rejection properties as the driver circuit 1 is bipolar.

The second path 7 and the fourth path 9 are provided with respective current sensors 14 and 15 for sensing the charging and the discharge current flowing into and out of the load 2. The first sensor 14 detects the charging current when the load 2 is
15 charged with negative polarity through the second charging circuit formed by the second and third paths 7 and 8. Similarly, the second sensor 15 detects the charging current when the load 2 is charged through the first charging circuit formed by the first path 6 and fourth path 9. Both detectors 14 and 15 detect the discharge current through the discharge circuit formed by the second and fourth paths 7 and 9. The
20 sensors 14 and 15 may be any suitable current sensors, for example a small resistor associated with a voltage sensor to detect the potential difference across the resistor. The sensors 14 and 15 may be positioned on either side of the switches S_2 and S_4 in the second and third paths 7 and 8, respectively.

The controller 12 controls the switches S_1 to S_4 to control switching of the
25 charging and discharge circuits in response to both the input signal V_{IN} and the output voltage V_{OUT} across the load 2 detected by the detector 13 as the output signal on the load 2. In particular, the controller 12 controls switching to drive the output voltage V_{OUT} in accordance with the input signal V_{IN} . The controller 12 also controls the switching of the charging circuit and discharge circuit in response to the current
30 flowing into and out of the load 2 detected by the sensors 14 and 15.

-12-

The manner in which the controller 12 controls the switching of S_1 to S_4 will now be described. To aid understanding, first a general description will be given, followed by a description of a specific algorithm which may be implemented by the controller 12.

5 First there will be described the operation of the controller when the input signal

V_{IN} is of positive polarity.

When the controller 12 detects that the output voltage V_{OUT} is below the input signal V_{IN} , so that charging of the load 2 is required, the controller controls the
10 switches from S_1 to S_4 to switch the driver circuit 1 alternatively between two states which will be called State 1 and State 2. In State 1, the first charging circuit formed by the first path 6 and the fourth path 9 is closed by closing switches S_1 and S_4 whilst opening switches S_2 and S_3 . In State 2, the first charging circuit is opened by opening switch S_1 and the discharge circuit formed by the second path 7 and the fourth path 9
15 is closed by closing switches S_2 and S_4 . Switch S_3 remains open. The resulting output voltage V_{OUT} and charging current I_C are illustrated in Fig. 2.

In State 1, the load 2 is charged by the PSU 3 through the inductor 5. Accordingly, the charging current I_C rises at a rate limited by the inductance of the inductor 5. At the same time, the charging current charges the load 2 so the output
20 voltage V_{OUT} also rises. State 1 is maintained until the controller 12 detects that the charging current I_C has risen to a predetermined maximum charging current $I_{C_{MAX}}$. Then the controller switches the driver circuit 1 to State 2.

In State 2, the charging circuit is open so the PSU 3 is no longer connected across the load 2. However, the inductor 5 continues to drive the charging current I_C
25 as it is not possible to instantaneously change the current flowing through an inductor. The discharge circuit is closed in State 2 to provide a path for the continuing charging current driven by the inductor 5.

In State 2, the charging current falls, the rate of fall being limited by the inductance of the inductor 5. During this time the output voltage V_{OUT} continues to
30 rise, but at a decreasing rate. State 2 is maintained until the controller 12 detects that

-13-

the charging current has fallen to a predetermined minimum charging current I_{CMIN} . Then the controller 12 switches the driver circuit 1 back to State 1.

In this way, the controller 2 cycles the driver circuit 1 alternately between States 1 and 2 until the output voltage V_{OUT} is driven to reach the input signal V_{IN} .

5 Thus, during State 1 energy is transferred from the PSU 3 to the inductor 5 and the load 2 and during State 2 the energy stored by the inductor 5 is transferred to the load 2 driven by the inductor 5. During this cycle, the current flow is limited below the maximum charging current I_{CMAX} . Accordingly, the power dissipated in the residual resistance of the driver circuit 1 is similarly maintained at a low level.

10 When the controller 12 determines that the output voltage V_{OUT} is above the input signal V_{IN} so that discharge of the load 2 is required, the controller 12 controls the switches S_1 to S_4 to switch the driver circuit 1 alternatively between two further states which will be called State 3 and State 4. In State 3, the discharge circuit formed by the second path 7 and the fourth path 9 is closed by closing the switches
15 S_2 and S_4 whilst opening switches S_1 and S_3 . In State 4, the discharge circuit is opened by opening switch S_2 , but the charging path formed by the first path 6 and the fourth path 9 is closed by closing the switch S_1 and maintaining the switch S_4 closed.

As far as the state of the switches S_1 and S_4 are concerned, States 3 and 4 are the same as States 2 and 1, respectively. However, States 3 and 4 differ from States
20 1 and 2 in how the output voltage V_{OUT} and the discharge current I_{D} varies. This is now described and is illustrated in Fig. 3.

In State 3, the discharge current rises at a rate limited by the inductance of the inductor 5. At the same time, the output voltage V_{OUT} falls. State 3 is maintained until the controller 12 detects that the discharge current I_{D} reaches a predetermined
25 maximum discharge current I_{DMAX} . Then, the controller 12 switches the driver circuit 1 to State 4. In State 4, the discharge current I_{D} continues to flow driven by the inductor 5, because it is not possible to instantaneously change the current flowing through an inductor. The charging circuit formed by the first path 6 and fourth path 9 is closed to provide a path for the discharge current back into the PSU 3 against the
30 potential of the PSU 3. The nature of the inductor 5 is that the internal stored

-14-

magnetic energy causes a terminal voltage to be generated across the inductor 5 which is sufficient to allow the discharge current I_D to flow against the potential of the PSU 3. Thus, the inductor 5 forces current back into the PSU 3. In other words, the energy stored in the inductor 5 is transferred back to the PSU 3 where it may be stored for future use. The overall effect is for the energy stored in the load 2 to be transferred to the inductor during State 3 and to be transferred during State 4 back into the PSU 3 driven by the inductor 5. This transferral of energy from the load 2 back to the PSU 3, by the inductor 5, means that the energy stored by the load 2 is in most part returned to the PSU 3 instead of being dissipated as heat and wasted. Of course, there will be some power wastage caused by dissipation in the residual resistance of the driver circuit 1, but this is limited by the fact that the discharge current I_D is itself limited to be below $I_{D\text{MAX}}$.

State 4 is maintained until the discharge I_D falls until the controller 12 detects that the discharge I_D has fallen to a predetermined minimum discharge current $I_{D\text{MIN}}$. Then, the controller 12 switches the driver circuit 1 back to State 3.

In this way, the driver circuit 2 is alternately switched between States 3 and 4 until controller 12 detects that the output voltage V_{OUT} has been driven down to the level of the input signal V_{IN} .

In practice, as the charging current I_C and the discharge current I_D are limited during charging and discharge of the load 2, the energy dissipated in the residual resistance of the driver circuit 1 is maintained at a low level. In practice, it is possible to achieve energy losses of only a few percent.

The above description of the control affected by controller 12 relates to the situation that the input signal is of positive polarity. Of course, the driver circuit 1 is bipolar, so can drive the output voltage to a negative polarity when the input signal V_{IN} falls below zero. In this case, the controller 12 controls the switches S_1 to S_4 to switch the driver circuit 1 in the exactly the same manner as described above except that closure of the second charging circuit formed by the second path 7 and the third path 8 (by closing switches S_2 and S_3) for charging the load to negative polarity replaces closure of the first charging path formed by the first path 6 and the fourth

-15-

path 9 (by closing switched S_1 and S_4) in States 1 and 4 described above. The discharge circuit is still formed by the second path 7 and the fourth path 9 and is closed in the same manner by closing switches S_2 and S_4 , as in States 2 and 3 described above. Of course the charging and discharge currents flow in the opposite
5 direction.

Fig. 4 is a flow chart of a specific algorithm which may be implemented in the controller 12 to effect the switching described in general terms above.

After starting, the algorithm proceeds to step 20 which determines whether the input signal V_{IN} is of positive polarity. If so, the control algorithm proceeds to step
10 21.

In step 21, it is determined whether input signal V_{IN} is above the output signal V_{OUT} (or more specifically if the magnitude of the input signal V_{IN} exceeds the magnitude of the output signal V_{OUT}). If so, the control algorithm proceeds to step 22. In step 22, the controller 12 sets the state of the switches S_1 to S_4 to State 1.

15 The control algorithm proceeds to step 23 where it is determined whether the charging current I_C exceeds the maximum charging $I_{C_{MAX}}$. If not, the control algorithm returns to step 20. As a result the algorithm cycles through steps 20 to 23 and drive circuit 1 is maintained in State 1 until the charging current I_C exceeds the predetermined maximum current $I_{C_{MAX}}$ (or a change detected in step 20 or 21 as
20 further discussed below).

When step 23 determines that the charging current I_C does exceed the predetermined maximum charging current $I_{C_{MAX}}$ the control algorithm proceeds to step 24 in which the controller 12 sets the switches S_1 to S_4 to put the driver circuit 1 in State 2.

25 After this, the controller algorithm proceeds to step 25 where it is determined whether the charging current I_C is less than the minimum charging current $I_{C_{MIN}}$. If not, the algorithm goes back to step 25 via steps 30 and 31 which are identical to steps 20 and 21, respectively. Steps 30 and 31 are provided to ensure the driver circuit 1 does not remain in State 2 if the input signal V_{IN} changes polarity or
30 discharge is required. If no change is detected in steps 30 and 31, then step 25 is

-16-

repeated until the changing current I_C is less than the minimum charging current $I_{C\text{MIN}}$, during which time the driver circuit 1 is maintained in State 2. Then, the control algorithm returns to Step 20 and, provided no change is determined in steps 20 and 21, the driver circuit is switched back to State 1 in step 23. Therefore, the control
5 algorithm causes the driver circuit 1 to alternate between States 1 and 2 until a change is detected in steps 20 or 21.

When it is determined in either of steps 21 or 31 that the output voltage is below the input signal the V_{IN} , the control algorithm proceeds to step 26 where the controller 12 switches the driver circuit 1 to State 3. Then the control algorithm
10 proceeds to step 27 where it is determined whether the discharge current I_D exceeds the predetermined maximum discharge current $I_{D\text{MAX}}$. If not, the control algorithm returns to step 20 and hence, provided no change is detected in steps 20 and 21, returns to step 26 maintaining the driver circuit in State 3.

When step 27 detects that the discharge current exceeds the predetermined
15 maximum discharge current $I_{D\text{MAX}}$, the control algorithm proceeds to step 28 where the controller 12 controls the switches S1 to S4 to switch the driver circuit 1 to State 4. The control algorithm proceeds to step 29 where it is determined whether the discharge current I_D has fallen below the predetermined minimum discharge current $I_{D\text{MIN}}$. If not, the algorithm goes back to step 29 via steps 32 and 33 which are
20 identical to steps 20 and 21, respectively. Steps 32 and 33 are provided to ensure the driver circuit 1 does not remain in State 4 if the input signal V_{IN} changes polarity or charging is required. If it is determined in step 33 that the input signal V_{IN} exceeds the output signal V_{OUT} , then the algorithm returns to step 22 as described above. If no change is detected in steps 32 and 33, then step 29 is repeated maintaining the driver
25 circuit in State 4 until it is determined that the discharge current I_D has fallen below the predetermined minimum discharge current $I_{D\text{MIN}}$. Then the control algorithm returns to step 20 and, provided no change has been detected in steps 20 or 21, the control algorithm proceeds to step 26 so the controller 12 puts the driver circuit 1 into State 3. In this way, the control algorithm causes the control 12 to switch the driver
30 circuit 1 between States 3 and 4 until a change is detected in steps 20 or 21.

-17-

When any of steps 20, 30 or 32 detect that the input signal is of negative polarity, the control algorithm proceeds to 34 to 46. Step 34 to 46 are identical to steps 21 to 33, respectively, except that (1) the various voltages and currents are of opposite polarity with appropriate changes to the signs in the decision steps, and (2) the States set in steps 35 and 41, corresponding to steps 22 and 28, in which the charging circuit is closed, involve closing the second charging circuit formed by the second path 7 and the third path 8 by closing switches S_2 and S_3 and opening switches S_1 and S_4 , instead of closing the first charging circuit formed by the first and fourth paths 6 and 9.

The controller 12 may be any control and monitoring circuit suitable for implementing the algorithm illustrated in Fig. 4. In a preferred form, the controller 12 is a programmable logic device, but could equally be a microprocessor or a digital signal processor. When the power driver circuit 1 is implemented in a device such as a mobile telephone where a microprocessor or digital signal processor is already present for performing other functions, this could be used as the controller 12 of the present invention.

The predetermined maximum and minimum charging and discharge currents may be selected or controlled as follows. The maximum charging and discharge currents $I_{C\text{MAX}}$ and $I_{D\text{MAX}}$, which are not necessarily equal, are selected to control the resolution of the cycling of the driver circuit 1 between States 1 and 2 and between States 3 and 4, having regard to the expected frequency range of the input signal V_{IN} . In particular, the lower the predetermined maximum currents $I_{C\text{MAX}}$ and $I_{D\text{MAX}}$, the higher the resolution. The predetermined maximum currents $I_{C\text{MAX}}$ and $I_{D\text{MAX}}$ are also selected to be sufficiently low to protect the components of the driver circuit 1 from excessive current.

The predetermined minimum charging and discharge currents $I_{C\text{MIN}}$ and $I_{D\text{MIN}}$, which are not necessarily equal, can in general be any value below the predetermined maximum charging and discharge currents $I_{C\text{MAX}}$ and $I_{D\text{MAX}}$, respectively. The driver circuit 1 still works if the predetermined minimum currents $I_{C\text{MIN}}$ and $I_{D\text{MIN}}$ have negative values. However, this is less desirable as it causes the load 2 to be

-18-

discharged for a part of the charging cycle and similarly to be charged for a part of the discharge cycle. Therefore it is preferable that the minimum charging currents $I_{C\text{MIN}}$ and $I_{D\text{MIN}}$ are around zero or above, typically at the smallest measurable amount. Alternatively, the minimum charging current $I_{C\text{MIN}}$ and $I_{D\text{MIN}}$ may be set at a value
5 which is a substantial fraction of the maximum charging current $I_{C\text{MAX}}$ and $I_{D\text{MAX}}$, so that the average charging current I_C and discharge current I_D is increased, because the average current will be approximately half the sum of the maximum and minimum currents. This improves the frequency response of the driver circuit 1, because the average charging current I_C and discharge current I_D control the maximum rate of
10 change of the output voltage V_{OUT} .

Furthermore the maximum and minimum charging and discharge currents may be controlled to have varying levels based on the error between the input signal V_{IN} and the output voltage V_{OUT} using conventional control theory techniques.

As described above, the driver circuit 1 forces energy stored on the load 2
15 back into the PSU 3 against the output potential of the PSU 3. The reservoir capacitor 4 is provided as a reservoir for the stored charged forced back to the PSU 3 to assist in the storage of this charge, for example in the case that the PSU 3 is of a type which cannot receive a back current. Thus the reservoir capacitor 4 is optional in the case that the
20 PSU 3 is able to accept such charge. The reservoir capacitor 4 may be integral with the PSU 3. Where the PSU 3 is in the form of a battery, such as a number of NiCd cells, then no reservoir capacitor is needed at all (either internally or externally of the PSU 3) as the battery is directly capable of receiving and storing energy from the driver circuit 1.

25 Desirably, the total output capacitance C_O formed by the combination of the PSU 3 and the reservoir capacitor 4, if present, is significantly larger than the capacitance of the capacitive load 2. This is so that the voltage change caused by the transfer of charge back to the PSU 3 is an insignificant fraction of the output voltage of the PSU 3. The fractional change in the output voltage of the PSU 3 will be equal
30 to the square root of the ratio of the capacitance C_L of the load 2 to the output

-19-

capacitance C_R in accordance with the equation $dV/V = \sqrt{C_L/C_R}$. For example if the output capacitance C_R is of the order of a thousand times the capacitance C_L the load 2, then the fractional change in voltage is of the order of about 3%.

The energy stored in the inductor 5 as a fraction of the energy stored in the load 2 defines the resolution of the control cycle with respect to the frequency of the input signal V_{IN} . Desirably, to obtain a fine resolution, the inductor 5 has an inductance such that the impedance of the inductor 5 is at least an order of magnitude less than the impedance of the load 2 at an expected maximum frequency of the input signal V_{IN} . This is equivalent to requiring that the resonant frequency of the LC circuit formed by the inductor 5 and the load 2 is of an order of magnitude greater than the maximum frequency of the input signal V_{IN} .

Preferably, the internal resistance of the inductor 5 is at least an order of magnitude less than the impedance of the inductor 5 at the expected maximum frequency of the input signal V_{IN} . This ensures that the resistance of the inductor 5 is small relative to the impedance of the inductor 5, so that current is limited in a non-dissipative manner which minimises power loss in the inherent resistance of the inductor 5.

In the driver circuit 1 described above, the PSU 3 and the load 2 are considered to be part of the driver circuit 1. However, the driver circuit 1 may be manufactured separately from the PSU 3 and the load 2 and provided with terminals for subsequent attachment of the PSU 3 and the load 2. In this way, the driver circuit 1 may be used with a variety of different types of PSU 3 and a variety of different loads 2. Similarly, the driver circuit 1 may be provided with a terminal for receiving the input signal V_{IN} .

Numerous variations and modifications of the driver circuit 1 are envisaged. For example, the layout of the driver circuit 1 may be greatly changed provided that there is a switchable charging circuit for charging the load 2 from the PSU 3 and a switchable discharge circuit for discharging the load 2. As a simple alternative to forming the discharge circuit from the second and fourth paths 7 and 9, it is possible to form the discharge circuit from the first path 6 and the third path 9 by closing

-20-

switches S_1 and S_3 whilst opening switches S_2 and S_4 . This may be done at any point during the control algorithm where the discharge circuit is closed, but requires appropriate positioning of current sensors. More complex changes in the layout of the driver circuit 1 are possible. The charging circuits and discharge circuit may be
5 formed by common paths and components as in the driver circuit 1 of Fig. 1, or may be formed by separate paths and components. The location and type of the current sensors 14 and 15 and voltage detector 13 may be freely changed.

Another variation is for the controller 12 to be arranged to control a characteristic of the load 2 other than the voltage across the load 2 as the output signal
10 which is controlled in accordance with the input signal V_{IN} . It is particularly advantageous for the controller 12 to control the charge stored by the load 2 as the output signal. This is achieved, for example in the driver circuits 51 and 61 shown in Figs. 5 and 6 respectively.

In the driver circuit 51 of Fig. 5, the detector 13 for detecting the voltage
15 across the load 2 is removed and an integrator 40 arranged to integrate the charging and discharge currents detected by the sensors 14 and 15 is added. The output of the integrator 40 thus is equal to the charge stored by the load 2, so the sensors 14 and 15 and the integrator 40 may together be considered to form a detector for detecting the charge stored by the load 2. Alternatively, the function of the integrator 40 may be
20 performed by the controller.

In the driver circuit 61 of Fig. 6, a detection capacitor 60 is arranged in series with the load 2 and the voltage across the detection capacitor 60 is measured by a voltage detector 62 which supplies the detected voltage to the controller. The detection capacitor 60 is charged by the charge flowing through it into and out of the
25 load 2 and effectively integrates the charge according to Kirchoff's equation. Therefore the voltage across the detector 62 is a measure of the charge stored on the load.

In both driver circuits 51 and 61 of Figs. 5 and 6 respectively, the controller 12 uses the stored charge as the output signal of the load 2, instead of the voltage
30 across the load 2. Otherwise, the capacitive discharge circuits 51 and 61 of Figs. 5

-21-

and 6 are identical to that of Fig. 1 and the control effected by the controller 12 is identical to that described above, so a description thereof is not repeated. As a result, the controller 12 causes the charge stored across the load to be controlled in accordance with the input signal V_{IN} . This is particularly advantageous in the case of
5 a load 2 which is a piezoelectric or other electro-active device in which the displacement of the device is non-linear with the applied voltage, but is linear with the applied charge. Thus it becomes possible to control the displacement of the device in accordance with the input signal which is not possible if the power driver circuit drives the voltage across the load 2 as the output signal.

10 Instead of the detectors 13 or 40 to detect the output signal, the driver circuit 1 could include an estimator to estimate the output signal based on the detected current and a knowledge of the capacitance of the load and the ratings of the other components of the driver circuit 1. In that case, the estimator would serve as the means for deriving a measure of the output signal.

15 Similarly, instead of the sensors 14 and 15, the driver circuit could include an estimator to estimate the current flowing based on the detected output voltage and a knowledge of the load and other components of the driver circuit 1. Such an estimator would be able to raise or lower the current flowing through the load to its desired maximum or minimum, by calculation or knowing the values in the
20 relationship

$\delta i / \delta t = E / L$, where E is the potential across the inductor, L and $\delta i / \delta t$ is the rate of change in the current. The potential across the inductor can be calculated from knowing the supply voltage across the driver circuit and the voltage across the load. L and E are known by design. Then, for a desired change in the current through the
25 load, the switches can be configured to either charge or discharge, or recycle for a calculated period of time δt to achieve the desired change in current δi . In the algorithm illustrated in Fig. 4, the decisions based on measurements of the current would be replaced by decision boxes that have decrementing times, whose initial value is estimated by the estimator current.

30

-22-

CLAIMS

1. A capacitive power driver circuit for driving an output signal on a capacitive load in accordance with an input signal, the driver circuit comprising:
 - 5 a switchable charging circuit for charging the load from a power supply unit;
 - a switchable discharge circuit for discharging the load;
 - an inductor in series with the load in the charging circuit and the discharge circuit;
 - means for deriving a measure of the output signal on the load; and
 - 10 a controller, responsive to the input signal and the derived output signal, for controlling switching of the charging circuit and discharge circuit to drive the output signal in accordance with the input signal.
2. A capacitive power drive circuit according to claim 1, wherein
 - 15 the driver circuit further comprises at least one current sensor for detecting the current flowing into and out of the load, and
 - the controller is responsive to the current detected by the at least one current sensor to control said switching.
- 20 3. A capacitive power drive circuit according to claims 1 or 2, wherein the controller is arranged during charging of the load to switch alternately between: closing the charging circuit; and opening the charging circuit while closing the discharge circuit to provide a path for the charging current driven by the inductor.
- 25 4. A capacitive power drive circuit according to claim 3, wherein the controller is arranged during charging of the load to switch from closing the charging circuit to opening the charging circuit in response to the magnitude of the charging current rising to a predetermined maximum charging current.
- 30 5. A capacitive power drive circuit according to claim 4, wherein the controller

-23-

is arranged during charging of the load to switch from opening the charging circuit to closing the charging circuit in response to the charging current falling to a predetermined minimum charging current.

- 5 6. A capacitive power drive circuit according to claims 4 or 5, wherein the controller is arranged to vary the predetermined maximum and/or minimum charging currents in response to the magnitude of the difference between the input signal or output signal.
- 10 7. A capacitive power driver according to any one of claims 4 to 6, wherein the controller is arranged during charging of the load to maintain a positive charging current.
8. A capacitive power drive circuit according to any one of the preceding claims,
15 wherein the controller is arranged during discharging of the load to switch alternately between: closing the discharge circuit; and opening the discharge circuit while closing the charging circuit for the discharge current to be driven by the inductor into the power supply unit against the output potential of the power supply unit.
- 20 9. A capacitive power drive circuit according to claim 8, wherein the controller is arranged during discharging of the load to switch from closing the discharge circuit to opening the discharge circuit in response to the magnitude of the discharge current rising to a predetermined maximum discharge current.
- 25 10. A capacitive power drive circuit according to claim 9, wherein the controller is arranged during discharging of the load to switch from opening the discharge circuit to closing the discharge circuit in response to the discharge current falling to a predetermined minimum discharge current.
- 30 11. A capacitive power drive circuit according to claims 9 or 10, wherein the

-24-

controller is arranged to vary the predetermined maximum and/or minimum discharging currents in response to the magnitude of the difference between the input signal or output signal.

- 5 12. A capacitive power driver according to any one of claims 8 to 11, wherein the controller is arranged during discharging of the load to maintain a positive discharge current.
- 10 13. A capacitive power drive circuit according to any one of the preceding claims, wherein the charging circuit is a bipolar circuit for selectively charging the load from the power supply unit in either polarity.
- 15 14. A capacitive power drive circuit according to claim 13, wherein the charging circuit comprises a bridge arrangement of four paths around the series arrangement of the inductor and the load, the first and second paths switchable connecting respective outputs of the power supply unit to one end of the series arrangement of the inductor and the load and the third and fourth paths switchable connecting respective outputs of the power supply unit to the other end of the series arrangement of the inductor and the load, whereby the first and fourth paths comprise a charging path for charging the load with one polarity and the second and third paths comprise a charging path for charging the load with the opposite polarity.
- 20 15. A capacitive power drive circuit according to claim 14, wherein two of the four paths connected to the same output of the power supply unit are switchable connected together to form the discharge circuit.
- 25 16. A capacitive power drive circuit according to claim 15, wherein each path includes a switch for selectively opening and closing the path, the controller being arranged to control the switches.

-25-

17. A capacitive power drive circuit according to any one of the preceding claims, wherein the means for deriving is a detector for detecting the output signal on the load.
- 5 18. A capacitive power drive circuit according to claim 17, wherein the detector is for detecting the output signal as the voltage across the load.
19. A capacitive power drive circuit according to claim 17, wherein the detector is for detecting the output signal as the charge stored by the load.
- 10 20. A capacitive power drive circuit according to claim 19, wherein the detector includes a current sensor for detecting the current flowing into and out of the load and means for integrating the detected current to derive the charge stored by the load.
- 15 21. A capacitive power driver circuit according to claim 19, wherein the detector includes a detection capacitor arranged to be charged by the current flowing into and out of the load and means for detecting the voltage across the detection capacitor.
- 20 22. A capacitive power driver according to claim 21, wherein the detection capacitor is arranged in series with the load.
23. A capacitive power drive circuit according to any one of the preceding claims, further comprising a reservoir capacitor in parallel with the power supply unit.
- 25 24. A capacitive power drive circuit according to claim 23, wherein the capacitance of the reservoir capacitor is at least an order of magnitude larger than the capacitance of the load.
- 30 25. A capacitive power drive circuit according to any one of the preceding claims, wherein the inductor is of a type having an insignificant energy loss.

-26-

26. A capacitive power drive circuit according to any one of the preceding claims, wherein the internal resistance of the inductor is at least an order of magnitude less than the impedance of the inductor at an expected maximum frequency of the input signal.

5

27. A capacitive power drive circuit according to any one of the preceding claims, wherein the inductor has an inductance such that the impedance of the inductor is at least an order of magnitude less than the impedance of a predetermined load at an expected maximum frequency of the input signal.

10

28. A capacitive power driver circuit for driving an output signal on a capacitive load in accordance with an input signal, the driver circuit comprising:

a switchable charging circuit for charging the load from a power supply unit;
a switchable discharge circuit for discharging the load;

15

a detector for detecting the charge stored by the load as the output signal on the load; and

a controller, responsive to the input signal and the output signal detected by the detector, for controlling switching of the charging circuit and discharge circuit to drive the output signal in accordance with the input signal.

20

29. A capacitive power drive circuit according to claim 28, wherein the detector includes a current sensor for detecting the current flowing into and out of the load and means for integrating the detected current to derive the charge stored by the load.

25

30. A capacitive power driver circuit according to claim 29, wherein the detector includes a detection capacitor arranged to be charged by the current flowing into and out of the load and means for detecting the voltage across the detection capacitor.

31. A capacitive power driver according to claim 30, wherein the detection capacitor is arranged in series with the load.

30

1/4

Fig.1.

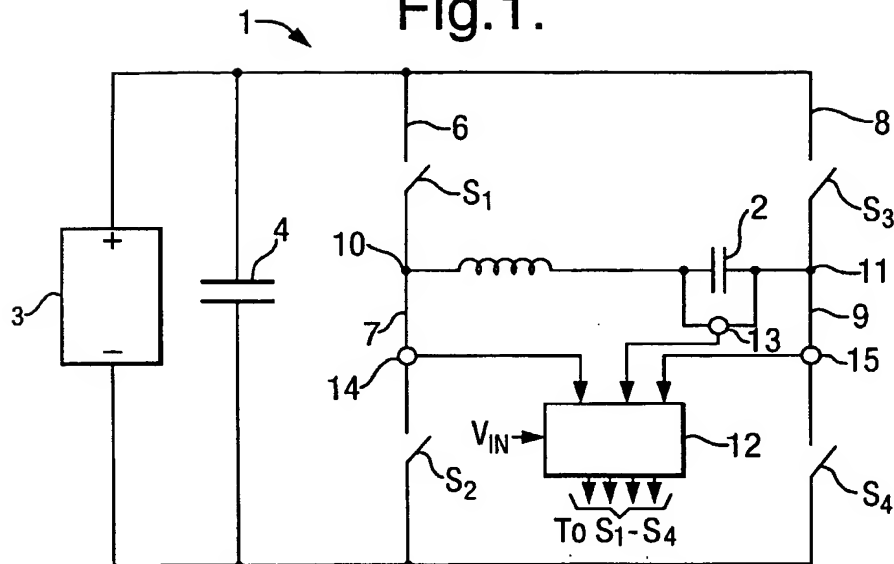


Fig.2.

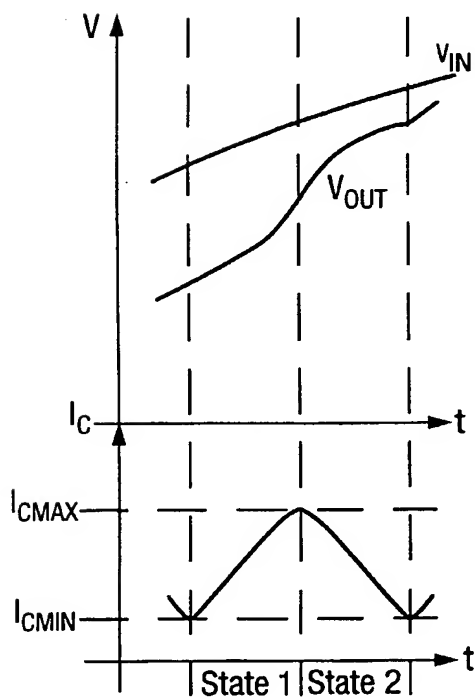


Fig.3.

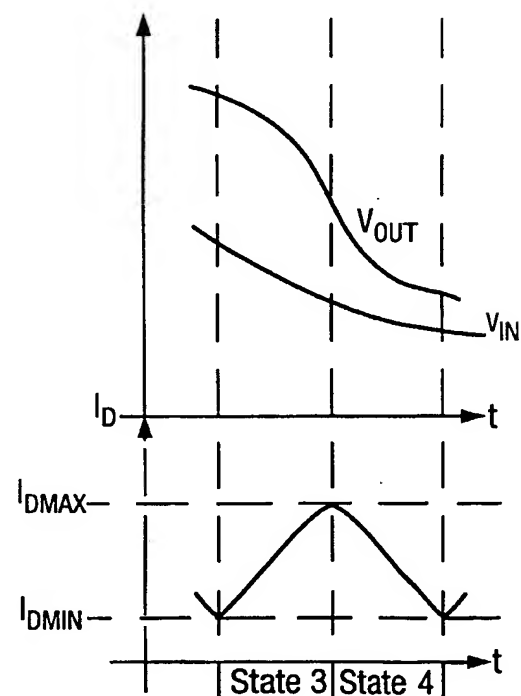
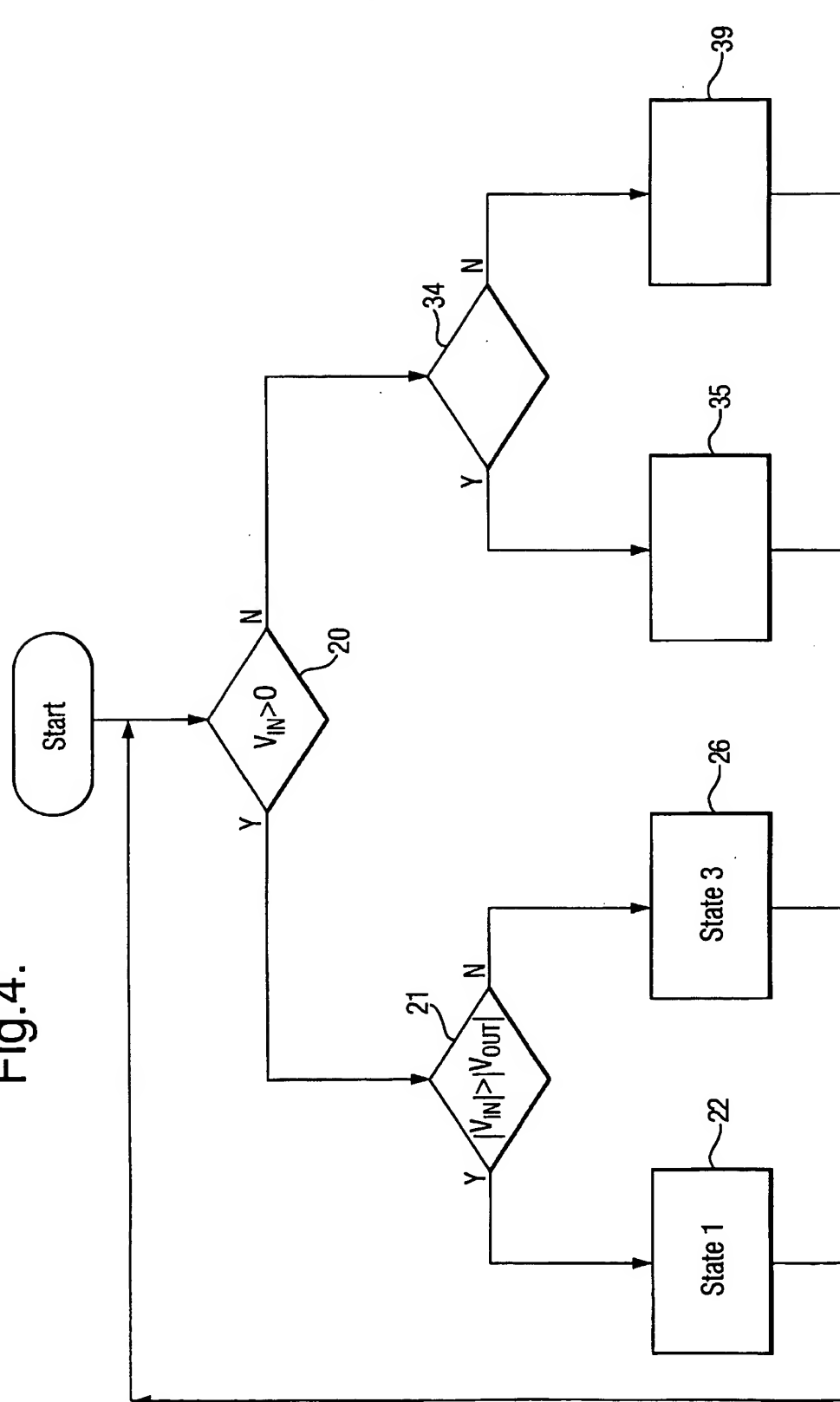
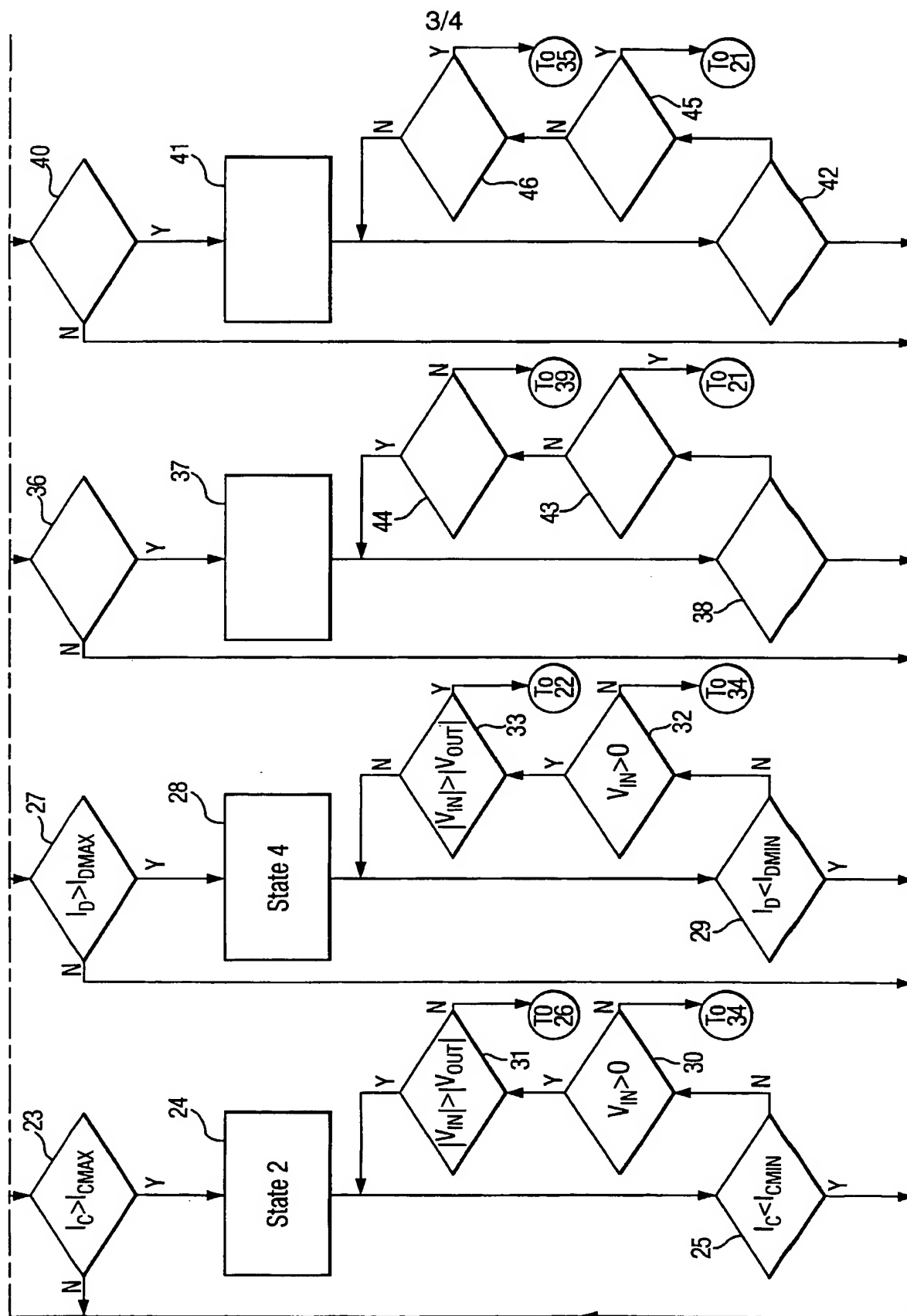


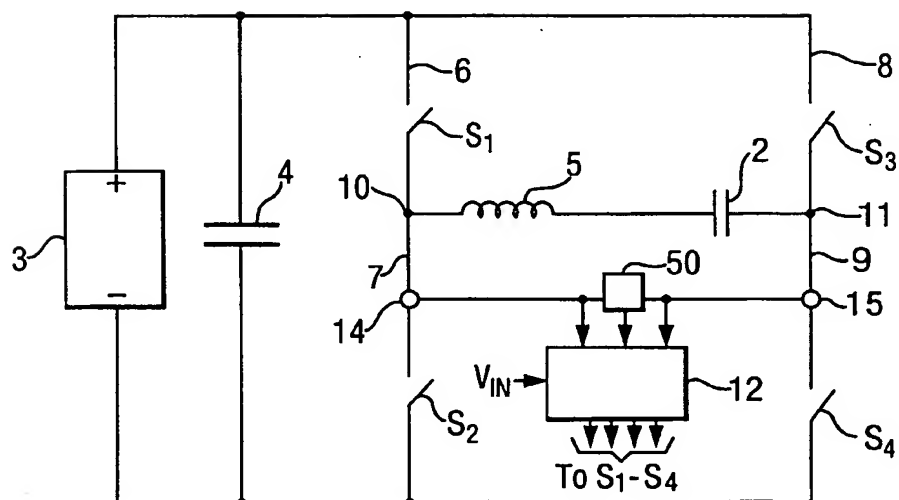
Fig.4.





4/4

51 Fig.5.



61 Fig.6.

